Implementing an Enhanced Tool Kit for Modular Portable Lab Kit for Logic Design

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***Abstract*— Introduction to Logic Design, a perquisite course for many engineering disciplines, is an intensive theory and hands on class. The hand-ons aspects requires hardware for experiencing building and testing of logic circuits. On-line sections require the ability of students to work completely off campus. This paper presents various tools to enhance the student's Logic Lab experience and rate of success.**

Keywords - Remote Laboratories, STEM Education, on-line Classes, on-line Laboratories, Virtual Laboratories.

I. Introduction

Continued growth of Engineering Lab courses along with the additional requirement to support students on-line. New Tools and techniques are required to address the expanding the scope of modernizing Logic Labs. [1]

This paper presents methodologies to address these issues: Working with color blind students, refining the logic probe circuit, learning hexadecimal, Resolving queue for grading & help requests, and methods to discouraging cheating.

II. Physical Lab Access Opportunities

The Department of Computer and Electrical Engineering and Computer Science (CEECS) at Florida Atlantic University (FAU), uses a shared lab space method to allow for more efficient space utilization and more Teaching Assistant (TA) contact time. Three classes utilize the 60 bench lab: Logic Design lab (250-300 students), Microprocessor (150-200 students) and Embedded Systems (60 students). The lab is open 24 / 7 via magnetic card, TAs are in the lab for approximately 40 hours a week. The Lab Assignment due dates are bi-weekly, the Microprocessor lab first due date is due 2 weeks in and Logic Design the 3rd week, Embedded Systems is an advanced class with the professor directly assisting the students 4-6 hours per week.

III. Meeting the Needs of Commuter and On-line Students

Eighty-Eight percent of students commute, the University serves a very large area over 150 miles by 50 miles. This large area requires alternate methods to deliver course content, one method is to provide more engineering courses on-line. There is a need to provide commuter and on-line students in engineering courses that involve a lab with a lab kit that they can use at home to build and test their logic circuits, for the on-line students, a way to have the labs graded without having to come on campus.[1] *"The need for development of remote, virtual and mobile labs has led the Education Society of the Institute of Electrical and Electronics Engineers (IEEE) to form a working group to develop standards for P1876 Networked Smart Learning Objects for on-line Laboratories"* [2] . There are various methods and models that can be used for mobile and on-line laboratories[3] .

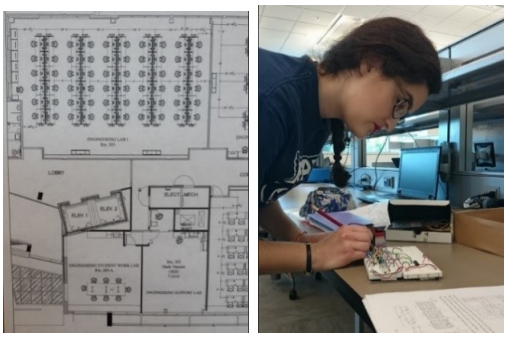

Fig. 1. (a) Floor plan (b) Student in lab with new lab kit
(a) By: FAU Planning (b) Used with Permission.

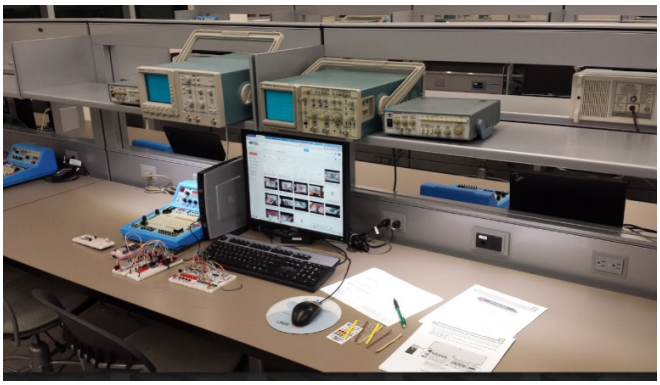

Fig. 2. Logic / Microprocessor / Embedded Lab setup (60 seats)

The FAU CEECS Lab Manager created instructional videos[14]-[28] to guide students as they progress through the beginning logic assignments. The videos[14]-[28] cover every aspect from explaining the function of each component, demonstrating the basic assembly and operation of a breadboard, wire stripping, IC pin straightening and how to

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assemble the Logic Labs infrastructure step-by-step including exact placement of each part. This was necessitated as this was the first time many students had seen a breadboard. Many students have not taken Physics 2 or Circuits 1 and were unprepared in the use of breadboards and/or electronics. [1]

IV. The Digital Logic Lab

"The digital logic design has been defined by IEEE and ACM societies as one of core areas."[2] Many universities use digital logic design as the gateway course to undergraduate computer science and computer & electrical engineering. In this paper we will focus on the methods and improvements to enhance the students experience for the Logic Design course. Our goal was to further develop the stand-alone, low cost, tether-less lab that students build themselves, requiring the physical lab for only extra help or grading. [1] and enhancing the in-lab student experience.

V. Working with colorblind students

During Lab orientation we inform colorblind students they will encounter difficulty with building the lab, and they should contact the Lab Manager to receive assistance on organizing their parts to facilitate easier construction. In the prior semesters we encountered one or two students, recently we have encountered six students with some level of difficulty of color differentiation. *"Complete color blindness or achromasy is rare, but weakness or absence of discrimination to certain colors can be found in at least 8% of the male population. The most useful description of these color defects is in terms of hue and saturation, thresholds ..."* [32] The most common issues is Red / Green or Blue / Yellow / Green, most see them as variations of gray.

Colorblind students would normally be encouraged to to select another engineering discipline, not requiring intensive use of colors such as mechanical or civil. With the movement to surface mount parts and automated tools e.g. color recognition cell phone apps. Students can perform well in the CEECS discipline.

The solution is to separate the parts and tape them down on a piece of paper and to write the values on the paper. Figure 3 This opens the opportunity to teach them students how to use a Digital Multi Meter (DMM). Once they have the learned to use the DMM their confidence and concern about perusing a career in Electrical / Computer Engineering / Computer Science is boosted. Most have returned to demonstrated their successful completion of the Portable Lab Kit.

VI. Second Portable Lab Kit (PLLK2)

The PLLK2 Includes: a robust battery-operated power supply, reverse polarity protection for the logic buses, LED status indicators, more DIP-switches, 4 push button switches, Tri-State logic probe, dual 7-segment display, and dual square wave oscillators. To keep the portable lab kit cost down, $20.15 [1]

The cost of kitting was eliminated by utilizing all TAs assigned to departmental courses to assemble and package

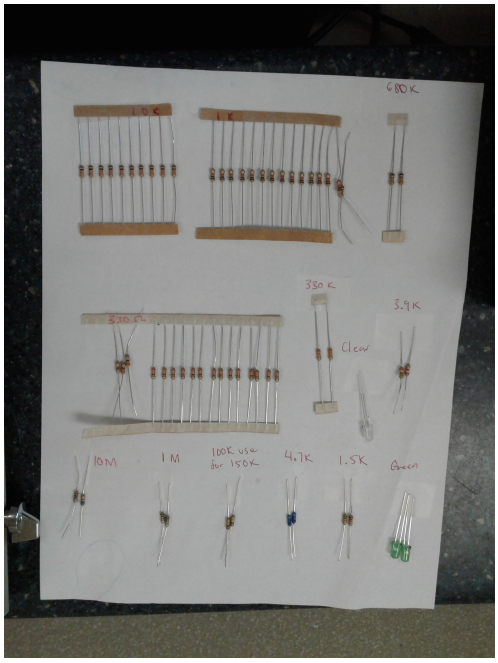

Fig. 3. Wired 2nd Portable Logic Lab Kit (PLLK2)

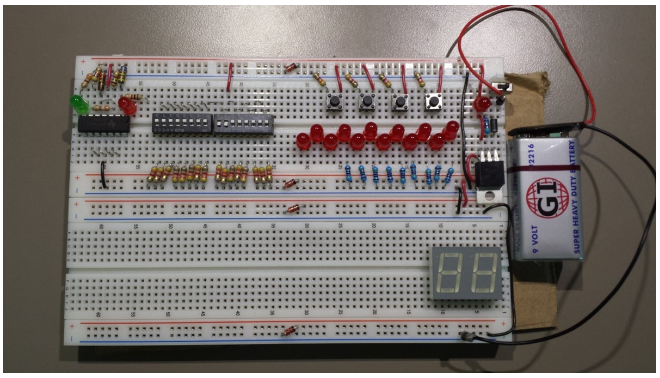

Fig. 4. Wired 2nd Portable Logic Lab Kit (PLLK2)

the kits the first week of classes, Figure: 5. The TAs build over 750 kits for all the classes with labs: Logic Design Microprocessors, Electronics Labs 1 & 2, Senior Design. They also build kits for the special offering classes with labs: Electromagnetic Compatibility, Summer Camp High School Electronics Lab, Hack-A-Thon, among others. [1]

To avoid having to mail replacement components to online students and to avoid component failure, we examined methods to "harden" the kit. Eliminating issues due to incorrect wiring, a diode protects against incorrect polarity of the 5V regulator (LM7805) . We added Zener diodes and capacitors to maintain a steadier 5V signal and prevent issues cause by connecting the 9V battery to the 5V bus, or worse connecting the 9V backwards to the 5V bus. To reduce student anxiety due to the increased analog components a set of videos[14]-[28] guides them step-by-step through the building of the infrastructure section of breadboard and testing of the NOT, AND, OR, and NAND chips as preparation

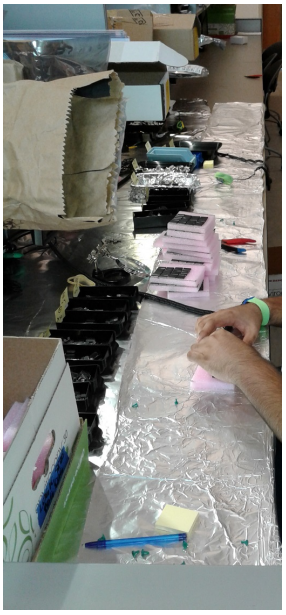

Fig. 5. A TA putting the ICs into anti-static foam

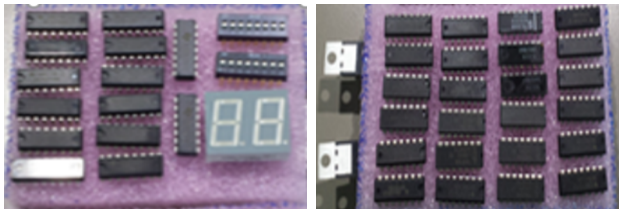

Fig. 6. PLLK2 Lab kit components distributed with breadboard and wire

to their orientation lab. [1]

The PLLK2 contains simpler, cheaper, and more durable parts; avoiding the issues caused by lack of parts knowledge shared by many of the students, RE: Physics 2. The PLLK2 provides 50% spare parts, double the total available breadboard size and includes a Tri-State logic probe for increased confidence while debugging, (Low=Red, High=Green, Off=Un-Connected), Figure 7. [1]

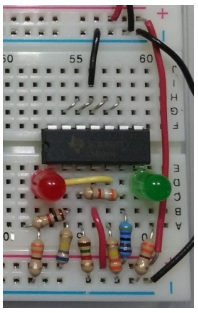

Fig. 7. PLLK2 Tri-State Logic Probe

Incorporating a Tri-State logic probe allows students to effectively troubleshoot their circuits and observe exactly how logic gates work, Figure 7. The substantial improvement in student confidence and success was worth the $0.75 cost. [1]

VII. Third Portable Lab Kit (PLLK3)

Applying two semesters of experience we upgraded the design: Adding a another LED to the Logic Probe to improve understanding of the third and most critical state while troubleshooting, Unconnected. Implemented a Hexadecimal Display Driver for teaching Binary and Base Sixteen. Minor part changes were also implemented: Replaced the LM324 for two LM358, Swapped the 74113 for the CMOS:4027.

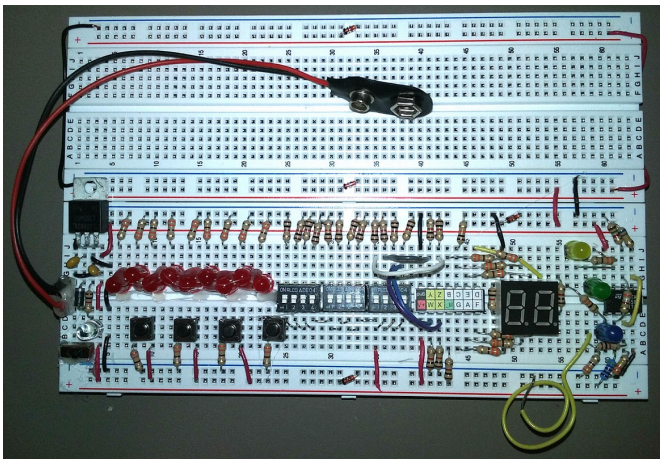

Fig. 8. PLLK3 Portable Logic Lab v3

The LM324 worked properly for approximately 98% students; those who followed the instructions and the videos. In later labs this part caused confusion since the power and ground are in the middle of the part: pins 4 & 11. Moving to the LM358 eliminated that confusion with power on the Top Right and Ground on the Bottom Left. The 74113 Dual JK Negative Edge Flip-Flop was a suboptimal choice, because the K was inverted and caused significant issues in creating the state tables.

Fig. 9. PLLK3 Parts

VIII. Improving the Logic Probe

When debugging about 10% of the students had trouble with the concept of no light means you have no connection.

2017s Intro Logic Design CDA 3201C, FAU, CEECS				
quan	part number	Pin out is the same for: LS,ALS,ACT,F,HCT,HC	Power Pins	Purpose
6	7400	Quad 2in NAND	Pin 14= + 7= --	Most Labs
3	7404	Hex Inverter	Pin 14= + 7= --	Most Labs
3	7408	Quad 2in AND	Pin 14= + 7= --	Most Labs
3	7410	Triple 3in NAND	Pin 14= + 7= --	Most Labs
3	7420	Dual 4in NAND	Pin 14= + 7= --	Most Labs
2	7432	Quad 2in OR	Pin 14= + 7= --	Most Labs
2	7474	Dual D Flip Flop	Pin 14= + 7= --	Lab 4 & 5
3	74138	3:8 Demultiplexer / Decoder	Pin 16= + 8= --	Lab 4 & 5
2	74157	Quad 2:4 Multiplexer / Encoder	Pin 16= + 8= --	Lab 6
1	74283	4bit Adder	Pin 16= + 8= --	Lab 2
2	cd4027	Dual J K Flip Flop	Pin 16= + 8= --	Lab 4 & 5
3	cd4510	Presettable BCD Up/Down Counter	Pin 16= + 8= --	Lab 6
1	cd4543	BCD to7-segment, Com Anode or Cathode	Pin 16= + 8= --	Lab 6
3	LM358	Op-Amp, DUAL	Pin 8= + 4= --	Probe
1	PIC16f505	MicroController - Binary to Hexadecimal	Pin 1= + 14= --	ALL
2	78m05	5v Voltage Regulator -- 500mA, TO-220	1=In 2=Gnd 3=Out	Power Supply
1	3622AH	LED Display, DUAL, 7-segment, 2-Cathodes	CC.L=10, CC.R=5	Lab 6
3	SW.DIP-04	Dip SW-04, Raised, Low Profile Body		All
4	PB.SW-n.o.	SWITCH, TACTILE SPST-NO 50mA		Lab 4 & 5
1	9V Battery Connector	9v clip w/ tinned wires	Red= + Black= --	Power Supply
9	LED.Red	LED, Red, T-1 3/4	Flat Side= "--"	Status
2	LED.Green	LED, Green, T-1 3/4	Flat Side= "--"	Probe
2	LED.Yellow	LED, Yellow, T-1 3/4	Flat Side= "--"	Probe
2	LED.Blue	LED, Blue, T-1 3/4	Flat Side= "--"	Probe
2	LED.White	LED, White, T-1 3/4	Flat Side= "--"	Power Supply
4	0.1uF Cap	0.1 uf 20% 50v capacitor		Power & Lab 6
25	330 Ohm 1/4W Resistor 5%	Orange Orange Brown Gold	PB Switches & LEDs *only*	
20	1.0k 1/4W Resistor 5%	Brown Black Red Gold	Switches & Probe	
2	1.5k 1/4W Resistor 5%	Brown Green Red Gold		Probe
2	3.9k 1/4W Resistor 5%	Orange White Red Gold		Probe
2	4.7k 1/4W Resistor 5%	Yellow Violet Red Gold		Probe
5	10k 1/4W Resistor 5%	Brown Black Orange Gold		Probe + Lab 6
2	330k 1/4W Resistor 5%	Orange Orange Yellow Gold		Probe
2	620k or 680k 1/4W @ 5%	Blue Red Yellow Gold -or- Blue Gray Yellow Gold		Probe
4	1M 1/4W Resistor 5%	Brown Black Green Gold		Lab 6
6	n751a or 1n5231a or 1n4733a	5.1v Zener Diode [Green, Black, Orange or White case]	Band=+5V **	Protection
2	1n4001 ... 1n4007	1amp Diode [Green or Black case]	Band= "--"	Protection
3	2n2222 or 2n3904 or pn2222	NPN Transistor, TO-92	1=Emitter, 2=Base, 3=Collector	Lab 6
1	Switch.SPST.slide	Slide Switch SPST		Power Supply
2		Breadboard 830 points		Connections
1		Anti-Static Mat - Pink Foam - "Bug Rug"		Protection
1		Anti-Static Foil Bag	Save and Use this Bag	Protection
2	FEET	10 Wires of 22ga, Assorted colors	see video & visit EE96.203	Connections

Fig. 10. PLLK3 Parts List

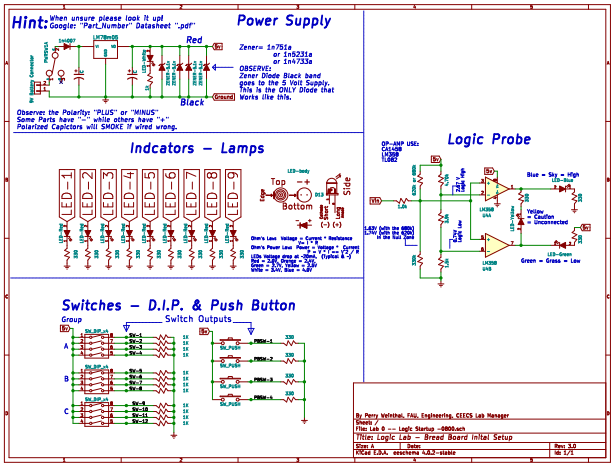

Fig. 11. Schematic for PLLK3, shown larger in the Appendix

Addressing this shortcoming with various lectures and videos HELPeD, the addition of one LED and a Resistor resolved the issue. We also changed the LEDs from RED Low and Green High because some students were confused with the main red LEDs indicating High. The Logic Probe indicates all three states visually: High (Blue), Low (Green) and Disconnected (Yellow). Figure 12 The Logic probe was implemented using the LM358 to reduce board real estate allowing for an the implementation of the Hexadecimal display.

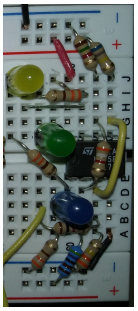

Fig. 12. PLLK3 Tri-State Logic Probe

IX. Hexadecimal Display

The choice to implement a sophisticated display driver was based on many factors: The need to display the Results from the 5 bit Adder Lab, The Microprocessor Professors lamented on how students failed to understand Base16. The introduction the concept of using micro-controllers as turnkey parts in projects.

Fig. 13. Wired 2nd Portable Logic Lab Kit (7447) [31]

The two common parts for driving a 7Segment display are the 7447 series (Common Cathode- 7446 Open Collector, 7447 Totem Pole Output; Common Anode 7448 Open Collector, 7449 Totem Pole Output) and the CD4543 (LCD / Common Anode / Common Cathode). The 7447 displays gibberish above 9, Figure 13 while the 4543 Blanks. The 7447 was designed very early in the 7400 product series and was optimized to take advantage of don't care states for a reduced gate count.

After investigating the options of implementing a Hexadecimal to Seven Segment display driver, the TIL311[29] is a very nice device for USD$25[30], unfortunately that is the total budget for the Logic Lab Kit.

The Hexadecimal Display was implemented using a 14pin PIC Micro-Controller (PIC), Figure 18. The original code was for the PIC16f1825, using a less sophisticated algorithm it was possible to implement on the PIC16f505 USD$0.68 part replacing the Non-Hexadecimal the CD4543 (USD$0.26) BCD to 7Segment display driver. After sourcing issues with the PIC16f505 we have settled on the PIC16f1503 USD$0.77. The parts are programmed by the TAs as part of the Kit Assembly process.

Students are able follow along the video while building this, where they learn to size the length of the parts and wires for efficient layout of the parts. Success was enhanced by the addition of a decal label showing EXACTLY where to connect the wire, Figure 18. Upon completion of this circuit students then demonstrate proper operation by testing all the

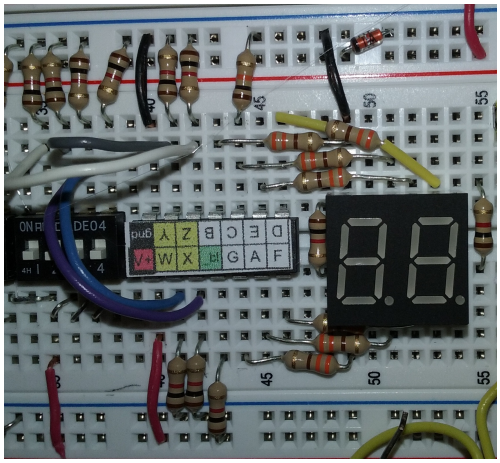

Fig. 14. Hexadecimal Display

states ”0” through ”F”, where they incidentally learn about Hexadecimal. Hexadecimal is further reinforced as they use the display as either the display to indicate inputs or outputs for all the labs they build. The cost to implement this was less than a USD$1.

The Hexadecimal Display Driver can be student ”configured” to accommodate either a Common Cathode or Common Anode type display, by placing a pull-up or pull-down resistor on the ”c” segment output. During the startup sequence the PIC code reads the state of the ”c” segment, Low is Common Cathode and High is Common Anode. If the display reads a ”-” for zero then the ”c” resistor is either not connected or in the wrong polarity. The PIC also reads the state ”g” segment for operating in Gray Code mode or Binary Mode, High is Gray Mode.

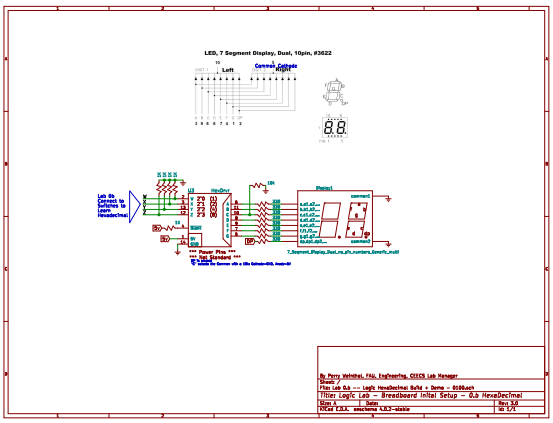

Fig. 15. Hexadecimal Schematic, shown larger in the appendix

X. Web-based Lab Queue for Grading and Help Requests

The original The Lab Queue was written on the white board in the front of the class. There were a few students that would write their name above the top of the queue while no one was watching ... leading to a few un-harmonious moments. Thus leading to the exploration of a better method for queuing. The Google Web-based queue is displayed on four large monitors in the Lab.[36] & [37]

Grading has a priority OVER Help,
Up to 10 people will be graded.* (*2 days prior to due date)

TA	Resolved / comments	Time-stamp	Class	Bench	Lab #	Name,
Chad	Yes	3/29/2018 20:59:49	Logic Grading	44	4	Julian
Chad	Yes	3/29/2018 21:09:57	Logic Grading	26	4	DANAILYS
Chad	Yes	3/29/2018 21:10:43	Logic Grading	25	4	LUGENIE
Chad	Yes	3/29/2018 21:15:21	Logic Grading	48	4	Anastasia
Chad	Yes	3/29/2018 21:20:08	Logic Grading	45	4	Said
Chad	Yes	3/29/2018 21:20:35	Logic Grading	36	3	Cedric
Chad	Not Needed	3/29/2018 21:24:49	Logic Help	12	4	Marlon
Chad	Yes	3/29/2018 21:25:26	Logic Grading	13	4	Dhaval
Chad	Not Ready	3/29/2018 21:31:15	Logic Grading	44	4	mahlik
Chad	Not Ready	3/29/2018 21:46:39	Logic Grading	22	4	Mincong
Chad	Yes	3/29/2018 21:48:40	Logic Grading	20	4	Hana
Chad	Yes	3/29/2018 21:57:10	Logic Grading	58	4	Blake
Chad	Yes	3/29/2018 22:04:15	Logic Grading	41	4	sam
Catalina	Yes	3/30/2018 9:34:11	Logic Help	33	5	jason
Catalina	Yes	3/30/2018 10:02:54	Micro Help	16	4	Rodrigo
Catalina	Yes	3/30/2018 10:43:49	Logic Help	33	5	jason
Catalina	Yes	3/30/2018 11:54:28	Micro Help	50	3	Patrick
Catalina	Yes	3/30/2018 11:57:46	Logic Help	16	3	Steven
Catalina	Yes	3/30/2018 12:11:15	Micro Grading	1	4	Dylan
Catalina	Yes	3/30/2018 12:18:03	Logic Grading	16	3	Steven
Catalina	Yes	3/30/2018 12:28:18	Micro Help	41	4	e
Catalina	Yes	3/30/2018 14:00:18	Micro Help	8	4	Rochelle
Mazhar	Yes	3/31/2018 10:32:44	Micro Grading	26	3	Kevin
Mazhar	Yes	3/31/2018 12:52:39	Micro Grading	29	3	FREDERIC
Mazhar	YES	3/31/2018 12:59:45	Micro Grading	28	3	Daniel
Mazhar	Yes	3/31/2018 13:16:31	Micro Help	29	3	FREDERIC
Mazhar	Yes	3/31/2018 15:55:20	Micro Help	40	3	Ryan
Mazhar	YEs	3/31/2018 16:27:33	Logic Grading	13	3	Chris
Mazhar	Yes	3/31/2018 17:07:11	Logic Help	16	3	Betsy

Fig. 16. Lab Queue

Improving the Lab Satisfaction and Reducing stress on both the student and the TAs by knowing where they are are in the queue and when they will be attended to, Figure 16 [37]. The data collected from this form is useful for determining the peak periods and scheduling TAs.

The TAs can only edit their name and resolution columns. Color coding green for grading and blue for help, with white text for Logic and black for Microprocessors improves readability. The use of the bench location allows the TAs to easily locate the students. Other info not displayed: student’s last name, email, id number. [37] The author has made the form and spreadsheet open for copying to your own account.

A later version will show the wait time statistics.

This semester the professors for Logic Design and Micro are reviewing the Lab Web Log to determine the ”effort” of students if they need the benefit of a point to ”bump” them into the next higher grade. If the students were working diligently in the labs and seeking help it is taken into consideration.

XI. Methods to Discourage Cheating and Plagiarism

Students who work & study diligently are adversely effected if the classes are curved they will receive lower overall grades to those whom behaved unethically. This affects student moral and the University’s reputation. We are finding test and assignments being posted on websites within a half hour of the release of an assignment. Students are very creative on ”sharing” their test problems during the

actual test. The University has a very stern view and strict policy on academic dishonesty. [6]

In the Labs we have tried many solutions, iteratively improving the method to deter issues. For example: A group of students shared a single finished breadboard and submitted that one unit, that lead to the required "pulling" of all the project wires. We HAD one TA that did not pull the wires if the students asked nicely, this lead to several students using this one TA and using the same project repeatedly. All students are now required to submit a photo of the finished lab with their ID in the picture. The professor was flummoxed by a cluster of students performing exceedingly well in the Labs and yet performing dismally on the exams. She reviewed the Lab images and found the same breadboard was summited for all of the poorly performing students and two other good students. The professor consulted with the two "good" students and learned they were sharing their work. All of those students were placed on academic probation.

With the on-line classes we have another issue since the students may be remote and many are local. We require they place their Student ID or Driver's License in the view of the camera while they record the demo of their project. Students are also required to video the pulling of the Lab wires at the end of the video.

We have the TAs enter the lab grade in the student's lab book grading sheet, one student claimed a TA failed to record his grades for two Labs in the grading spreadsheet. The TA became suspicious as he observed the "errant" TA's signature was of questionable pedigree, so he took a photo of the grade sheet. He showed it to the other TA and confirmed his suspicions. We followed up the with additional evidence of CCTV camera footage and the Lab Web Log, the student will be placed on academic probation.

While these methods help reduce plagiarism, only poor grades are the best end result, in this class failure to earnestly work in the lab will lead to inadequate performance on the exams.

XII. Future Improvements

Introducing a USB Input / Output with logic analyzer and analog input modes.

Web-based Lab Queue later version will show the wait time statistics.

Implement Hexadecimal Display Gray Code.

XIII. Conclusions

Portable Teaching Laboratories are a plausible low-cost solution for teaching on-site and remote / on-line classes. Students can achieve in-depth knowledge and develop skills when given reasonable supplemental materials to cover gaps in their knowledge of basic electronics. The availability of low cost tools and materials makes this possible. [1] The continued evolution of these labs will improve student knowledge and skills. On-line classes have been successfully accommodated using video conferencing and laboratory assignments can be graded by evaluating a video of the completed project uploaded by the student. There is a high class fill rate and retention. [1]

APPENDIX

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List of Figures

1 (a) Floor plan (b) Student in lab with new lab kit (a) By: FAU Planning (b) Used with Permission. 1
2 Logic / Microprocessor / Embedded Lab setup (60 seats) 1
3 Wired 2nd Portable Logic Lab Kit (PLLK2) . . 2
4 Wired 2nd Portable Logic Lab Kit (PLLK2) . . 2
5 A TA putting the ICs into anti-static foam . . . 3
6 PLLK2 Lab kit components distributed with breadboard and wire 3
7 PLLK2 Tri-State Logic Probe 3
8 PLLK3 Portable Logic Lab v3 3
9 PLLK3 Parts 3
10 PLLK3 Parts List 4
11 Schematic for PLLK3, shown larger in the Appendix 4
12 PLLK3 Tri-State Logic Probe 4
13 Wired 2nd Portable Logic Lab Kit (7447) [31] 4
14 Hexadecimal Display 5
15 Hexadecimal Schematic, shown larger in the appendix 5
16 Lab Queue 5
17 Schematic for PLLK3 8
18 Hexadecimal Schematic 9
19 Schematic for Lab6 10

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- 1a: By: FAU Planning
- 1b: Used with Permission.
- All others Drawings, Pictures & Tables by the Author: C. P. Weinthal

List of Tables

Tables by the Author: C. P. Weinthal

Contents

I Introduction 1

II Physical Lab Access Opportunities 1

III Meeting the Needs of Commuter and On-line Students 1

IV The Digital Logic Lab 2

V Working with colorblind students 2

VI Second Portable Lab Kit (PLLK2) 2

VII Third Portable Lab Kit (PLLK3) 3

VIII Improving the Logic Probe 3

IX Hexadecimal Display 4

X Web-based Lab Queue for Grading and Help Requests 5

XI Methods to Discourage Cheating and Plagiarism 5

XII Future Improvements 6

XIII Conclusions 6

References 6

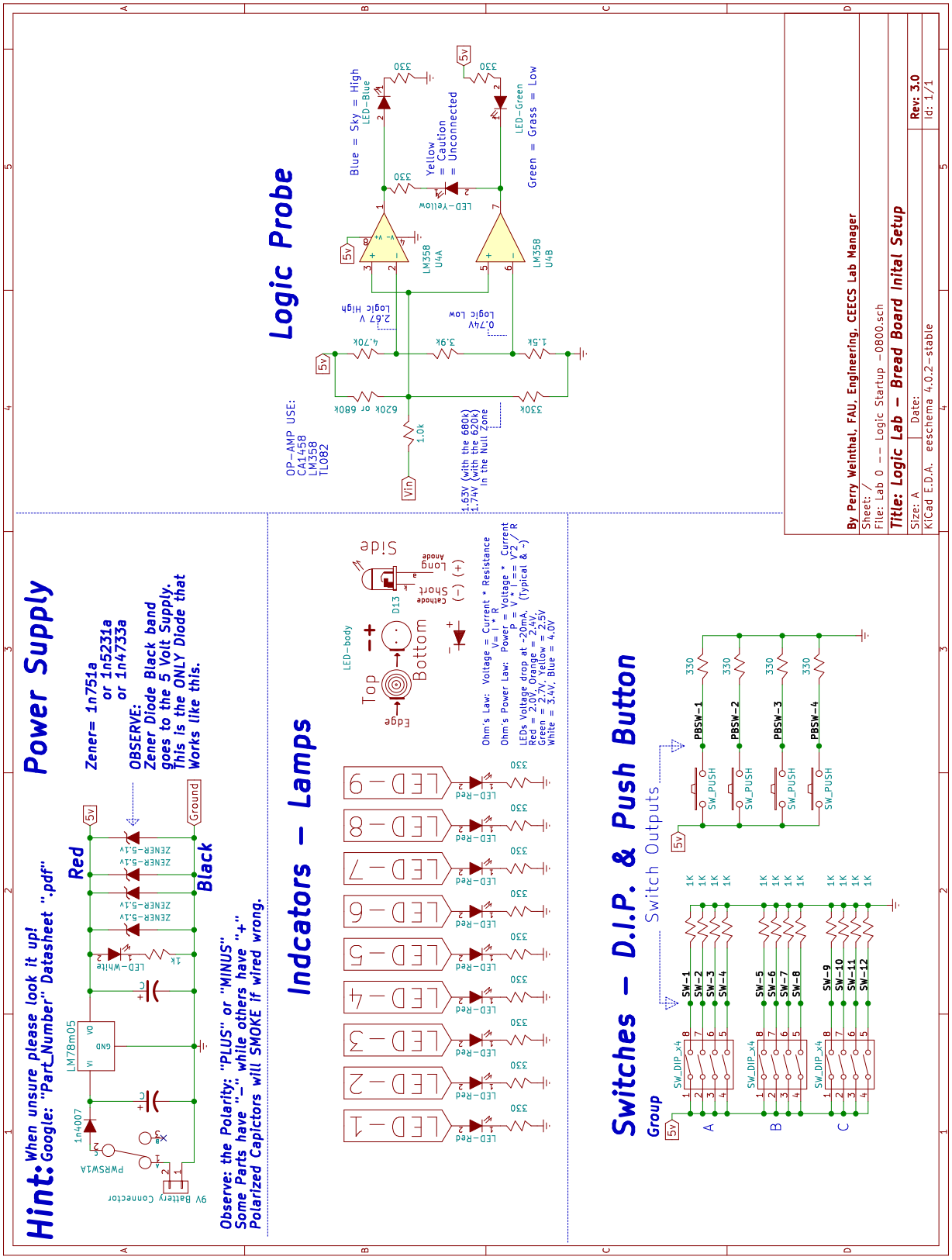

Fig. 17. Schematic for PLLK3

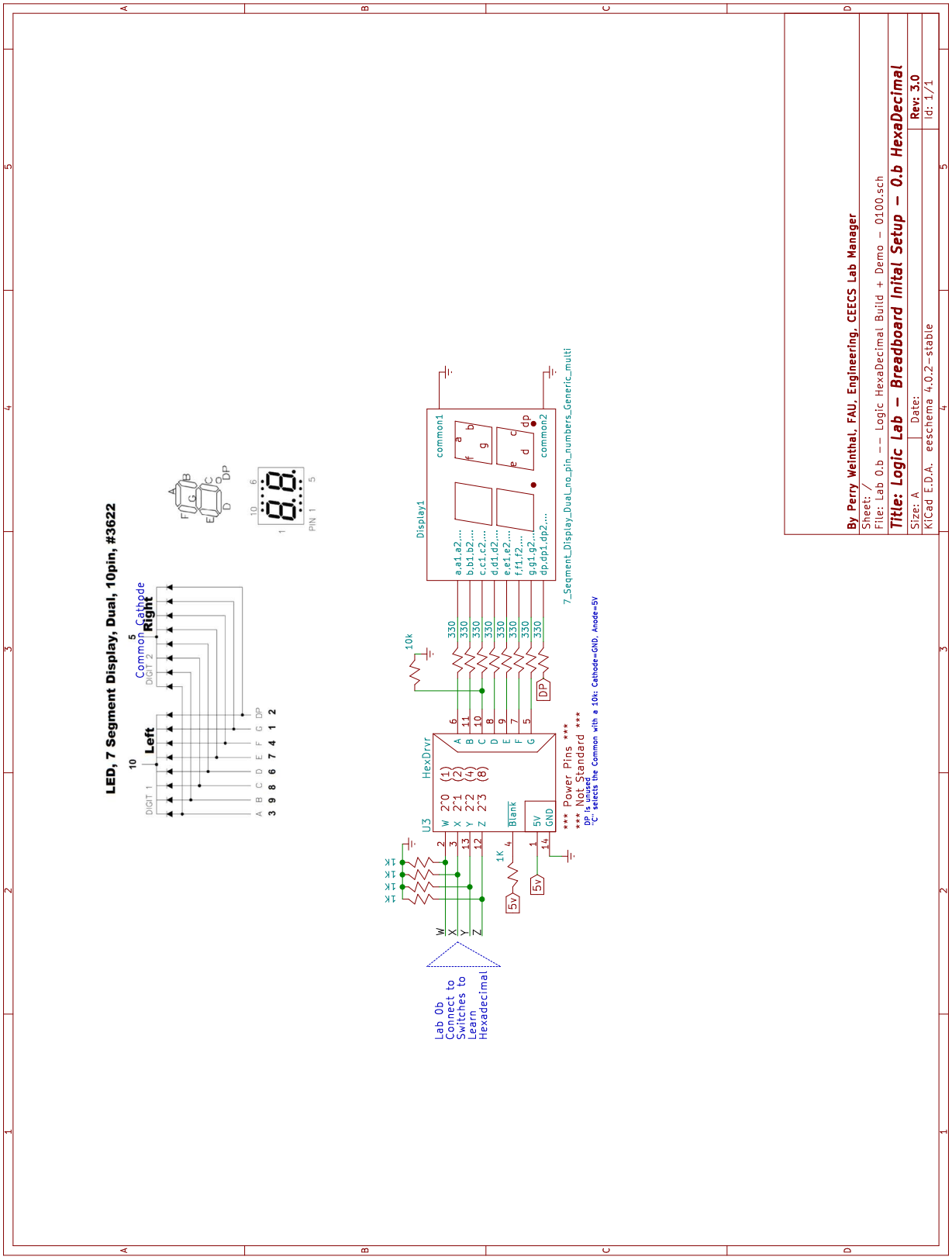

Fig. 18. Hexadecimal Schematic

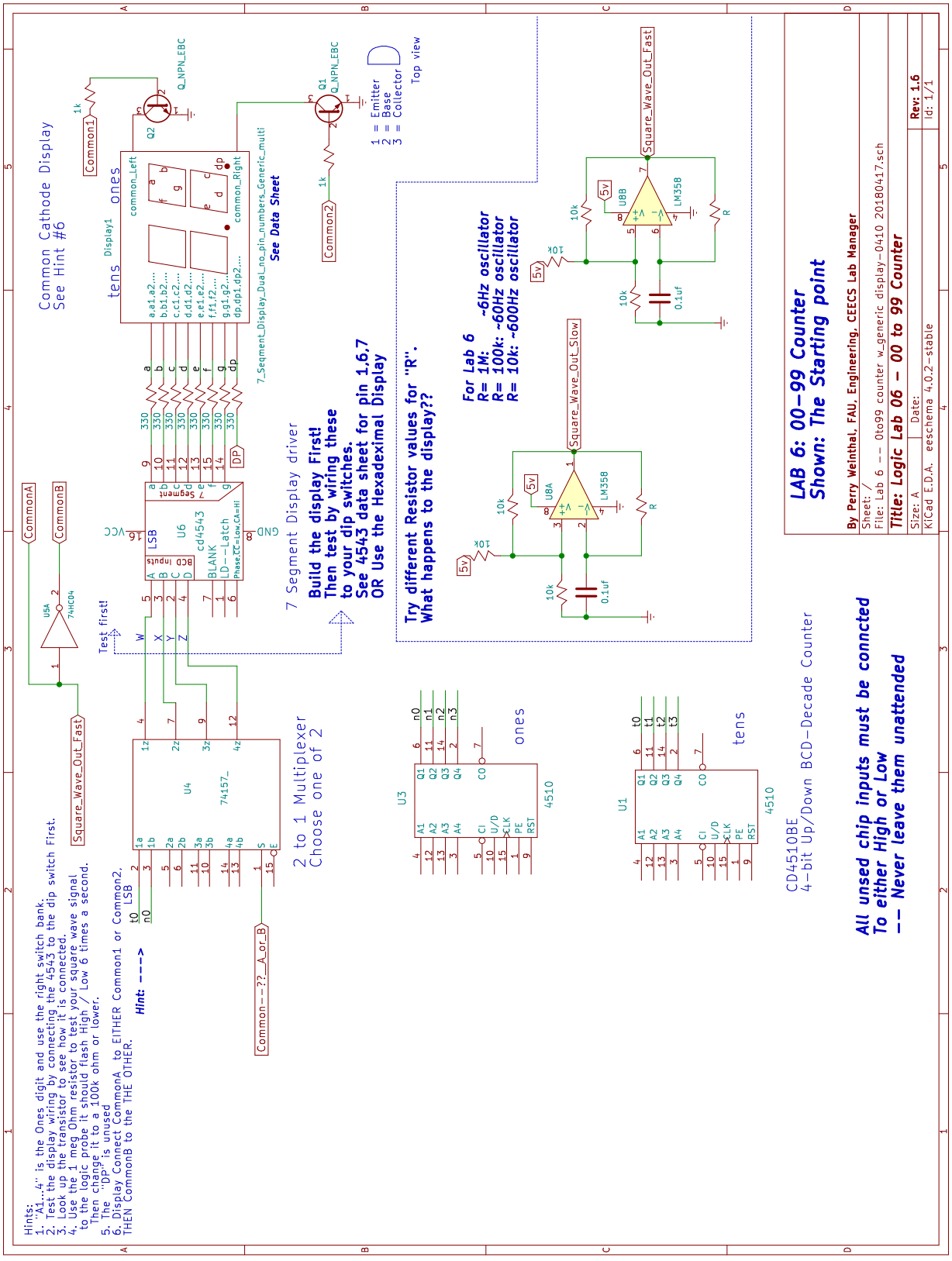

Fig. 19. Schematic for Lab6